# Buchchon (Poon) Bodhisuvarnachat

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## EDUCATION

**Carnegie Mellon University** | Pittsburgh, PA **Expected Graduation: December 2028**
Bachelor of Science in Electrical and Computer Engineering **GPA: 3.65**

- **Relevant Coursework:** Computer Systems, Principles of Imperative Computation, Discrete Mathematics
- **In Progress (Fall 26):** Digital Systems Design, Intro to Probability Theory, Intro to Engineering Entrepreneurship
- **Spring 27:** Logic Design & Verification, Embedded Systems, Parallel Computer Architecture and Programming

## EXPERIENCE

**Carnegie Mellon Racing (Formula SAE)**, Firmware, Controls, and Data Acquisition Engineer **August 2025 - Present**

- Co-lead the live telemetry module; migrating its link to the Particle Boron (LTE) from UART to SPI with COBS-framed CBOR messages, freeing the Boron's only UART to feed a Movella GNSS/INS for more precise GPS
- Validated MS4525DO differential pressure sensors for the pitot-tube aero sensing module using Raspberry Pi, verifying signal integrity and accuracy prior to hardware integration
- Profiled the driverless perception pipeline (TensorRT YOLO on Jetson AGX Orin) in NVIDIA Nsight Systems, decomposing the 6.5 ms per-frame latency budget across preprocessing, inference, and memory staging using NVTX ranges and GPU projection analysis
- Traced ~10% of per-frame time to GPU idle on pageable-memory image uploads moving at ~4% of available DRAM bandwidth; reviewed the diagnosis with the perception lead and logged it as a pipeline optimization item
- Instrumented a driverless MPPI controller's CUDA/Thrust pipeline with reusable CUDA events and NVTX ranges across noise generation, trajectory rollout, and reduction; added per-stage ns timing logs to identify GPU bottlenecks

**18-100 - Intro to Electrical and Computer Engineering**, Teaching Assistant **January 2026 - May 2026**

- Led weekly labs and recitations for 10 students, covering circuits, op-amps, digital logic, and microcontrollers

## PROJECTS

**Hardware Monte Carlo Option Pricer** | SystemVerilog, Python, cocotb, Verilator, Yosys/nextpnr **October 2026**

- Fully pipelined fixed-point Monte Carlo option pricer (1 path/cycle): xorshift RNGs, CLT Gaussian adder tree, block-RAM exp unit (2.6 LSB error); RTL within 2σ of Black-Scholes
- Sized the datapath with a fixed-point error sweep (rounding error 28× below Monte Carlo noise), uncovering a systematic rounding bias that grew as fractional bits were added
- Raised Fmax 61.6 → 89.1 MHz (+45%) on a Lattice ECP5 via critical-path pipelining, costing 69 flip-flops
- Verified every block bit-exact vs. Python models in cocotb: 9 tests, ~6,000 random vectors, 13 corner cases

**Aisle Be There (SteelHacks XIII Hackathon)**, Voice & Guidance Engineer **September 2026**

- iOS app guiding blind users through a full errand (team of 4, one weekend; React Native, Swift/ARKit)
- Owned the voice layer and fail-safes: 2-min handoff to store staff, no guessing on unverified WALK signals

**Computer Systems Labs (18-213)** | C **June - July 2026**

- Built a 64-bit malloc/free/realloc allocator (14-class segregated free lists, boundary-tag coalescing) scoring 100/100: 74.4% utilization at 8,936 Kops/s, up from 68.7% via footer elimination and 16-byte mini-blocks
- Built an LRU cache simulator (write-back/write-allocate, dirty-byte tracking) for arbitrary (s, E, b); cache-blocked matrix transpose (8×8, deferred diagonals) under full-credit miss thresholds on all three sizes

## SKILLS

- **Languages:** C, C++, Python, SystemVerilog, x86-64 Assembly, SQL
- **Hardware & Tools:** Verilator, cocotb, Yosys/nextpnr (Lattice ECP5), NVIDIA Nsight Systems, TensorRT, Jetson AGX Orin, SPI, UART, I²C, CAN, Raspberry Pi, Arduino, GDB, Git, Linux, AWS
- **Embedded & Lab**: STM32 (STM32CubeCLT, ST-LINK), CMake, oscilloscope, logic analyzer, multimeter